ally suited for MOS intra-well and bipolar intra-tub isolation. Shallow isolation element **40C** disposed over a single trench is ideally suited for densely packed bipolar active areas such as those employed in memory applications and CMOS inter-well isolation. In FIG. **18**, shallow isolation elements **40C** disposed over variable width trenches may be tailored depending upon the specific application for which they are intended. These variable width trenches allow for increased design flexibility.

To optimize CMOS inter-well isolation, mask **36** (see FIG. **13**) may be employed to form shallow isolation elements disposed over and extending beyond the edges of single, variable width trenches. In a BIMOS application, this would create a misregistration between shallow isolation elements in the bipolar regions and those in the MOS regions.

Thus it is apparent there has been provided, in accordance with the invention, an improved method of fabricating a semiconductor structure which meets the objects and advantages set forth above. While specific embodiments of the present invention have been shown and described, further modifications and improvements will occur to those skilled in the art. It is desired that it be understood, therefore, that this invention is not limited to the particular forms shown and it is intended in the appended claims to cover all modifications which do not depart from the spirit and scope of this invention.

What is claimed is:

1. A method of fabricating a semiconductor structure comprising the steps of:
- providing a semiconductor substrate;
- forming a thermal oxide layer on said substrate;
- forming a polycrystalline semiconductor layer on said thermal oxide layer;
- forming a first dielectric layer on said polycrystalline semiconductor layer;
- forming a first mask on said first dielectric layer and using said first mask to form at least one opening in said first dielectric layer, said at least one opening extending to said polycrystalline semiconductor layer;
- forming dielectric spacers in said at least one opening;
- forming a trench in said substrate beneath said at least one opening, said dielectric spacers creating a self-aligned reduction in the width of said trench;
- forming a dielectric trench liner in said trench and in said at least one opening;
- filling said trench with polycrystalline semiconductor material; and
- forming a shallow dielectric isolation element on said filled trench.

2. The method of claim **1** wherein the first dielectric layer comprises:
- a nitride layer formed on the polycrystalline semiconductor layer; and
- an oxide layer formed on said nitride layer.

3. The method of claim **2** further comprising the step of removing the dielectric spacers to create a self-aligned offset between the sidewall of the trench and the edge of the nitride layer to serve as a mask for the formation of the shallow dielectric isolation element.

4. The method of claim **2** wherein a dielectric cap is formed on the polycrystalline trench fill and combines with the dielectric trench liner to seal said polycrystalline trench fill.

5. The method of claim **4** wherein the oxide layer is removed prior to the formation of the dielectric cap.

6. The method of claim **1** wherein the first dielectric layer, the polycrystalline semiconductor layer, and the thermal oxide layer are completely removed following the formation of the shallow dielectric isolation element.

7. The method of claim **3** wherein the forming a first mask step includes using said first mask to form a plurality of openings in said first dielectric layer, the forming dielectric spacers step includes forming dielectric spacers in one or more of said openings, the forming a trench step includes forming a plurality of trenches beneath said plurality of openings wherein the width of said plurality of trenches is limited by said dielectric spacers if said dielectric spacers are formed in said openings corresponding to said trenches and the forming a shallow dielectric isolation element step includes forming a shallow dielectric isolation element on one or more of said trenches.

8. The method of claim **7** wherein the plurality of trenches are of approximately the same width.

9. The method of claim **7** wherein the plurality of trenches are of varying widths.

10. A method of fabricating a semiconductor structure comprising the steps of:
- providing a semiconductor substrate;
- forming a thermal oxide layer on said substrate;
- forming a polysilicon layer on said thermal oxide layer;
- forming a nitride layer on said polysilicon layer;
- forming an oxide layer on said nitride layer;
- forming a first mask on said oxide layer and using said first mask to form a plurality of openings extending to said polysilicon layer;
- forming dielectric spacers in said plurality of openings;
- forming trenches in said substrate beneath said plurality of openings, said dielectric spacers creating a self-aligned reduction in the widths of said trenches;
- removing said dielectric spacers to expose said polysilicon layer and create a self-aligned offset between the sidewalls of said trenches and the edge of said nitride layer;
- forming a dielectric trench liner in said plurality of trenches;
- filling said plurality of trenches with polysilicon so that said polysilicon in said plurality of trenches is substantially planar with said substrate;
- removing said oxide layer so that said nitride layer is exposed;
- forming a second mask on said nitride layer and using said second mask to form isolation element openings in said nitride layer; and
- forming shallow oxide isolation elements in said isolation element openings and also in those areas where said nitride layer was removed during the formation of said plurality of openings, said self-aligned offsets serving to limit the encroachment of said shallow oxide isolation elements formed therebetween.

11. The method of claim **10** wherein the removing said dielectric spacers step may be performed at various times between the forming trenches step and subsequent to the forming shallow oxide isolation elements step.

12. The method of claim **10** wherein a dielectric cap is formed on the polysilicon trench fill and combines with the dielectric trench liner to seal said polysilicon trench fill.